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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,494	12/19/2000	Kendell A. Chilton	EMC00-20(00124)	5725

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,494	CHILTON, KENDELL A.	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29,32-40 and 43-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29, 32-40, and 43-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 September 2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> --or--
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-29, 32-40, 43, and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Steinmetz et al. (6,425,034).

As per claims 1, 11, and 21, Steinmetz et al. teaches a fibre channel system including a host bus adapter 182 (figure 4; "interface") connected through a fibre channel FC 188 to a disk array controller 200 (figure 6; "volatile cache memory circuit") which includes a cache memory

210. The FC 188 represents a point-to-point channel between the host bus adaptor and the disk array controller. Shown in figures 3A and 3B are the read and write process between an initiator and target using the fibre channel protocol. An initiator (e.g. host through host bus adapter 182) sends a command to the target (e.g. cache of disk array controller 200). Data is transmitted between the initiator and target, the direction of data transmission depending upon whether the operation is a read or a write. Finally, status information is returned via a FCP_RSP sequence. See column 7, line 59, to column 8, line 16.

As per claims 2-4, 12-14, and 22-24, the fibre channel protocol includes unidirectional links as shown in figure 1B. All information passing from the host adapter to the disk array controller would pass through one set of wires (e.g. a command through the transmit wires) and all information passing from the disk array controller to the host adapter (e.g. status) would pass through the other set of wires (e.g. receive wires).

As per claims 5, 15, and 25, Steinmetz et al. teaches that the fibre channel protocol transmits data in units of frames. As shown in figure 2, the frames (for both reads and writes) include synchronization delimiters, such as "start-of-frame" and "end-of-frame".

As per claims 6, 16, and 26, Steinmetz et al. teaches that the fibre channel protocol transmits data in units of frames. As shown in figure 2, the frames (for both read and writes) includes CRC error check information.

As per claims 7, 17, and 27, Steinmetz et al. teaches read and write transactions as detailed above. Steinmetz et al. further teaches encoding the frames using the 8B/10B encoding/decoding scheme. See column 33, lines 20-38.

As per claims 8, 18, and 28, Steinmetz et al. teaches a busy signal at column 30, lines 1-2.

As per claims 9, 19-20 and 29, Steinmetz et al. teaches sending a frame header including an exchange identifier ("tag"). See column 6, lines 58-62.

As per claims 10 and 20, Steinmetz et al. teaches partitioning the sequence of read data if the data is larger than a frame. See column 7, lines 65-67. The multiple frames would be recombined at the host adapter ("processing the read data element").

As per claims 32-33, 36-37, and 39, Steinmetz et al. teaches transmitting and receiving multiple frames (see figure 3B, where A=1 and N=2).

As per claims 34-35, 38, and 40, Steinmetz et al. teaches sending a frame header including an exchange identifier ("tag"). See column 6, lines 58-62.

As per claims 43 and 45, Steinmetz et al. teaches that initiator (e.g. host through host bus adapter 182) sends a command to the target (e.g. cache of disk array controller 200). Data is transmitted between the initiator and target, the direction of data transmission depending upon whether the operation is a read or a write. Finally, status information is returned via a FCP_RSP sequence. See column 7, line 59, to column 8, line 16.

4. Claims 21 and 47 are rejected under 35 U.S.C. 102(b) as being anticipated by Ninomiya et al. (5,819,054).

As per claim 21, Ninomiya et al. teaches, with reference to figure 20, a storage system including a cache memory 203 ("volatile memory cache circuit") which caches data between a large scale disk and at least one host. Host adapters 201 interface the cache memory to the host(s) and disk adapters 202 interface the cache memory to the large scale disk ("an interface circuit"). A point-to-point channel directly connects the cache memory to each interface circuit.

As per claim 47, Ninomiya et al. teaches plural host adapters ("front-end interfaces") and plural disk adapters ("back-end interfaces"), each coupled to point-to-point interfaces.

5. Claims 1, 11, 21 and 43-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Thibault et al. (US 2003/0140192).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

It is further noted that the filing date of the 09/540,828 application is being relied upon in this rejection (figure 2 of the '192 publication and the '828 application are the same, and figure 8 of the '828 application corresponds to figure 5 of the '192 publication). Therefore, the effective filing date for figures 2 and 5 of the '192 publication is 31 March 2000, the filing date of the '828 application, of which the '192 is a continuation-in-part. It is noted that the '828 application also has the same assignee as the present application and the '192 publication.

As per claims 1 and 11, Thibault et al. teaches, with reference to figure 2, a system interface including a global cache memory 220 with a plurality of memory boards ("volatile memory cache circuit"), director 180 or 200 ("interface circuit"), and a plurality of point-to-point channels PTH directly connecting the directors to each memory board of the global cache memory. See figures 2 and 5. A read request is passed from a processor 121 to one or more of the front end directors 180 (paragraph [0039]), where a microprocessor makes a query

("command") from the global cache memory to determine if the desired data is located in the cache ("providing a command to the volatile memory cache circuit through the point-to-point channel which directly connects to both the interface circuit and the volatile memory cache circuit"; paragraph [0040]).

On a read hit, the data is transferred from the global cache memory 220 to the requesting processor over the point-to-point channel PTH ("moving a data element through the point-to-point channel in accordance with the command"). See paragraph [0040]. If the query of the cache results in read miss, then the front end director is informed such that it may then request the data from a disk drive ("receiving status from the volatile memory cache circuit through the point-to-point channel in accordance with the data element"). See paragraph [0041].

As per claim 21, Thibault et al. teaches, with reference to figure 2, a system interface including a global cache memory 220 ("volatile memory cache circuit"), director 180 or 200 ("interface circuit"), and a plurality of point-to-point connections PTH directly connecting the directors to the global cache memory.

As per claims 43 and 45, the cache memory boards immediately process the query to determine if the desired data is located therein.

As per claim 47, Thibault et al. teaches, with reference to figure 2, a plurality of front-end directors 180 connected to a plurality of processors 121 ("hosts") and a plurality of back-end directors 200 connected to a plurality of disk drives 141 ("non-volatile storage devices").

As per claims 44, 46, and 48, as shown in figure 5, there are a plurality of memory boards located between the front end directors and the back end directors (which are connected to the

disks), with point-to-point connections between each cache memory board and each director, thereby allowing concurrent operations

Response to Arguments

6. Applicant's arguments filed 23 September 2004 have been fully considered but they are not persuasive.

With respect to Applicant's arguments concerning the Steinmetz et al. reference (pages 17-20 of the response), Applicant argues that the FC 188 does not teach a point-to-point channel directly connecting the interface circuit and the volatile cache memory. In support of this Applicant indicates that the multi-drop PCI bus 208 of figure 6, connecting the FC controller 206 and cache memory 210 is not a direct point-to-point connection. However, as set forth in the rejection, the host bus adapter 182 (figure 4) represents the claimed "interface" and the disk array controller 200 (figure 6) represents the "volatile cache memory circuit". The fibre channel 188 interconnecting the host to the disk array controller represents the "direct point-to-point connection". See figures 1B, 3a-b, and 4 of Steinmetz et al.

It is noted that Applicant may consider the cache memory 210 of Steinmetz et al. to correspond to the claimed "volatile memory cache circuit". However, Applicant's "volatile memory cache circuit" is not limited to a cache memory alone, but also includes other elements. For example, as disclosed by Applicant, the "volatile memory cache circuit" includes interface circuitry and control circuitry in addition to "data element buffering circuitry" (i.e. a cache). See figure 4 and page 12, line 26 to page 13, line 7. This is similar to the disk array controller 200 of Steinmetz et al, which includes interface circuitry, control circuitry (microprocessor 212), and

the cache memory 210. Therefore, the disk array controller represents the "volatile memory cache circuit".

Conclusion

7. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(571) 273-4204**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (571) 272-4204. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (571) 272-4210.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
November 24, 2004